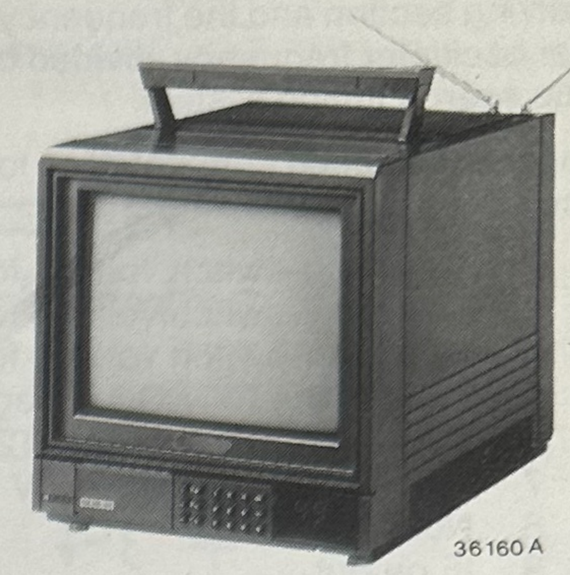
Service
Service
Service


36160A

Circuit Description

TABLE OF CONTENTS

Description des cicuits Schaltungsbeschreibung Kredsløbsbeskrivelse Kretsbeskrivelse Kretsbeskrivning Toimintaselostus Descrizione del circuito Description del circuito

GB
Subject to modification
4822 727 15149
Printed in The Netherlands
PHILIPS
Published by
Service Consumer Electronics
CS 98 295 GB

1. RF SECTION

Tuner U2211 contains the VHF receiving section, the UHF receiving section and the frequency divider which leads the tuner oscillator frequency, divided by 256, back to the automatic search tuning system.

The tuner has been connected as follows (see the complete circuit diagram):

Pin 2 12V band-switch voltage for band I
Pin 3 12V band-switch voltage for band III
Pin 4 12V band-switch voltage for UHF
Pin 5 Input of the RF-AGC voltage between 2 and 7,5 V
Pin 6 Operating voltage UB = 12 V
Pin 7 Tuning voltage UD 0-28 V
Pin 8 Not used
Pin 9 IF output
Pin 10 Not used

pl. 12 (plug 12)
Pin 1 Operating voltage 5 V for frequency divider.
Pin 2 FDIV, output of the oscillator frequency divided by 256:

$$\frac{(f_{osc})}{256}$$ (approx 0.5 V_{pp})

Pin 3 Ground

2. IF AMPLIFIER AND DETECTOR

The IF amplifier circuit is situated on the basic chassis. Use is made of a surface-wave filter and of the integrated circuit TDA3541 (see Fig. 2.1).

The IF signal arrives at the preamplifier stage with transistor T216 via input band filter L213/C213/R213, which is used for preselection. The pre-amplifier stage is a wide-band stage that operates with a gain factor V = 20, to compensate the losses of the subsequently applied surface wave filter. From collector T216, the amplified signal is supplied to the input, pin 1, of the surface-wave filter.

The surface-wave filter simulates the IF response curve and has specially been designed for intercarrier procedures; the sound rejection is approx. 26 dB.

The surface-wave filter supplies the selected IF signal to pins 1 and 16 of the integrated IF amplifier and demodulator circuit TDA3541.

The IF signal is amplified in three stages and rectified by the synchronous demodulator. The demodulator circuit is situated between pins 8 and 9 and has been trimmed for 38,9 MHz. Via the output amplifier, the CVBS signal arrives with 2,7 V_{pp} at pin 12, where the division into the CVBS signal and the 5,5 MHz sound information takes place (6 MHz for the PAL I system).TDA3541 contains an IF AGC. From this control the RF AGC has been derived which is available on pin 4. The inset point for the RF-AGC can be adjusted with potentiometer P221 (AGC Tuner).

3. SCART INTERFACE

3.1 CVBS signal path and change-over

Via pin 12 of the IF IC, the signal is fed, via the wave trap Q238/L238 and C239, to pin 3 of the switch-over IC TEA2014 (see Figure 2.1.).
An internal buffer circuit supplies the CVBS signal via pin 2 of TEA2014 to pin 19 of the EURO socket (CVBS output). The signal change-over switch, which has been built into TEA2014, is driven to pin 5 fo the IC by the switching voltage.

L-level signal path : pin 3 - pin 6
H-level signal path : pin 8 - pin 6

In this way the CVBS signal is present on pin 6 and pin 2 of TEA2014 if the TV is operating (AV switch not activated, no switching voltage on pin 8 of the EURO-socket). From pin 6, emitter follower T256 is triggered which applies the CVBS signal with 1 V_{pp} to pin 3 of connector 13 via a voltage divider. Connector 13 is equipped with a short-circuit connector.

3.2 Use of AV

When a signal source not having a switching voltage of its own is connected to the EURO socket, the CVBS signal on pin 20 of the EURO socket goes to pin 8 of TEA2014. When the key "AV on mann" on the rear cover of the set is depressed, a 12 V switching voltage is applied to the control input pin 5 of TEA2014. For processing in the set, the signal change-over switch applies the CVBS signal to pin 6 of TEA2014. In spite of the changed over signal change-over switch the RF section supplies during this time a CVBS signal to pin 19 of the EURO socket.
If external switching voltages are supplied, they are applied to the base of transistor T272. The transistor starts to conduct and drives T273 into conduction also, so that the 12 V switching voltage arrives on the control input, pin 5 of TEA2041 via D 261.
Via D097, T066 and D066, the switching voltage is fed to the synchronisation IC TDA2594, pin 13, to stop the change-over of the time constant.

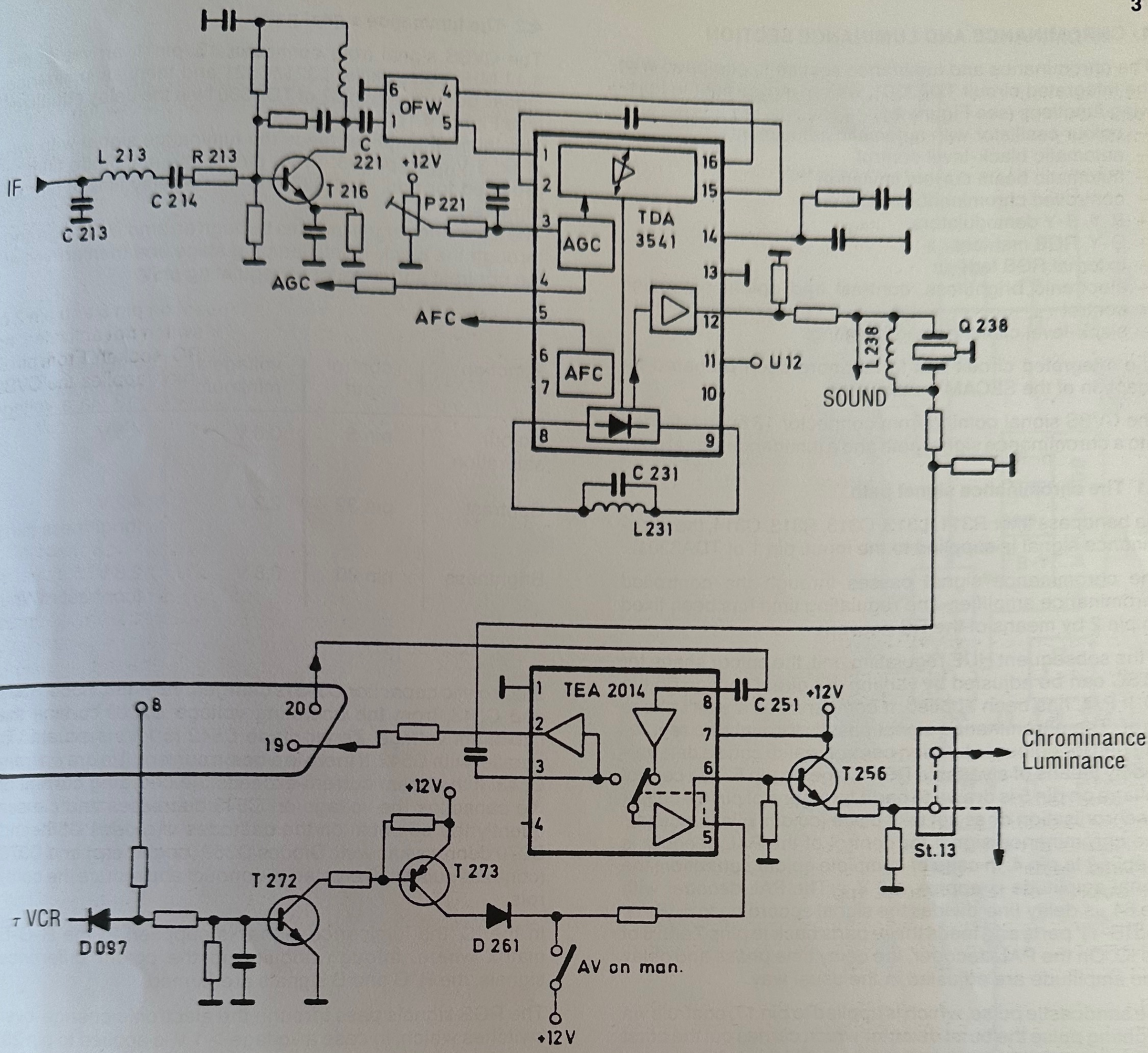

IF
L 213
R 213
C 213
C 214
T 216
C 221
OFW
+12V
P 221
AGC
AFC
TDA 3541
AGC
AFC
U 12
L 238
Q 238
SOUND
C 231
L 231
TEA 2014
C 251
+12V
T 256
Chrominance
Luminance
St. 13
T 272
T 273
VCR
D 097
D 261
AV on man.
+12V

Fig. 2.1

4. CHROMINANCE AND LUMINANCE SECTION

The chrominance and luminance section is equipped with the integrated circuit TDA3301, which carries out the following functions (see Figure 4.1):

- colour oscillator with automatic adjustment
- automatic black-level control
- automatic beam current limitation
- controlled chrominance amplifier
- R-Y, B-Y demodulators
- G-Y, RGB matrices
- external RGB fade-in
- electronic brightness, contrast and colour saturation control
- black-level clamping and blanking.

The integrated circuit has furthermore been prepared for adaption of the SECAM transcoders.

The CVBS signal coming from connector 13 is first divided into a chrominance signal path and a luminance signal path.

4.1 The chrominance signal path

Via bandpass filter R311, L313, C313, R313, C314, the chrominance signal is supplied to the input, pin 1 of TDA3301.

The chrominance signal passes through the controlled chrominance amplifier. The regulating time has been fixed on pin 2 by means of the RC network.

In the subsequent HUE regulating unit, the colour shade for NTSC can be adjusted by varying the direct voltage on pin 40. If PAL has been applied, it compensates a small phase error. The chrominance signal passes through the regulating unit for colour saturation control, which can be determined by means of a variable DC voltage on pin 5. The control voltage on pin 5 is drawn to earth by means of pin 5 if colour synchronisation does not take place (colour killer function). The chrominance signal for control of the PAL decoder is supplied to pin 4. In case of complete colour saturation, the signal amplitude is approx. 1,2 V_{pp}.The PAL decoder with the 64 μs delay line divides the signal according to $\pm$ (R-Y)' and (B-Y)' parts and feeds these parts back to pins 7 and 8 of the IC. On the PAL decoder, the delay time phase and delay time amplitude are adjusted in the usual way.

The sandcastle pulse, which is applied to pin 17, controls via its gating pulse the burst detector which carries out the burst gating and which synchronises the 4,43 MHz VCO (voltage controlled oscillator) via the H/2 circuit.
An external adjustment by means of a trimmer is not required anymore.

The synchronised 4,43 MHz oscillator acts directly as a control voltage for the (R-Y) synchronous demodulator and, via the PAL switch, as a control signal for the (B-Y) demodulator.

From both colour difference signals the G-Y signal is generated in the G-Y matrix. The three colour difference signals are fed to the matrix stages for RGB.

Servicing hint: by applying 12 V to pin 5, the chrominance signal path can be kept "open" without activating the colour killer.

4.2 The luminance signal path

The CVBS signal from connector 13, pin 1, arrives at the 4,43 MHz colour killer L321/C321 and then, as luminance signal, goes on to pin 37 of TDA3301 via the delay equalizer (see Figure 4.1).
The internal amplifier feeds the luminance signal with approx. 3 V_{pp} to pin 35. From pin 35 the amplitude filter is provided for and, via R337 and the Y-delay line of pin 36, triggered.
The luminance signal passes through an amplifier stage and through the black-level clamping stage and then arrives at the contrast and brightness regulating unit.

Function	control input	voltage at minimum	voltage at maximum
Colour saturation	pin 5	0,8 V	4,5 V
Contrast	pin 32	2,2 V	4,2 V (brightness min.)
Brightness	pin 30	0,8 V	2,8 V (contrast min.)

Electrolytic capacitor C543 is charged, via P366, R366, R369 and C543, from the operating voltage U200. To limit the maximum voltage, Zener diode D542 (5,1 V) is situated in parallel with C542. If there is a beam current, it is drawn from C543. If the beam current exceeds the charging current of the capacitor, the voltage on C543 decreases and consequently the potential on the cathodes of diodes D369 and D370 decrease as well. Diodes D369 (brightness) and D370 (contrast) successively start to conduct and reduce the controls.

In the IC, the luminance signal is supplied to the R-G-B matrix where, through addition to the colour difference signals, the R, G and B signals are formed.

The RGB signals pass through the electronic change-over switches which, in case a voltage > 1 V is applied to pin 23, switch over to pins 24, 25 and 26 and enable the reproduction of external RGB signals.
The switching steps also contain regulating units for contrast and brightness, so that external signals can be regulated as well.

Furthermore the integrated circuit TDA3301 contains an automatic black-level control which is not used, however, in this case.
The charging capacitors for this are situated on pins 15, 18 and 21. In order not to set the automatic black-level control into operation, the test inputs pin 16, 19 and 22 have been connected via resistors to the signal outputs.
Via pins 14, 17 and 20 and connector 11, the RGB signals are supplied to the picture tube PCB.

5. THE COLOUR OUTPUT STAGES

The three colour output stages are identical and are situated on the picture tube PCB. There is not an automatic black-level control. For this reason it was fairly easy to build up the output stages. Each of the three output stages consists of an emitter follower and an amplifier transistor.

The RGB signals are supplied to the picture tube PCB via connector 11. The signal amplitude is adjusted by means of white-level controls and is then fed to the subsequent emitter follower. The emitter followers enable a low-ohmic driving of the output stage transistors and, consequently, a reduction of the active Miller capacitance. At the same time, the emitter follower increases the base voltage. This facilitates the realization of the protection circuit and negative feedback.

The supply voltage is 160 V. The maximum modulations are 55 V_{pp}.

Black level adjustment takes place through changes of the emitter bias voltages. If the vertical deflection is absent, the V-flyback generator does not supply any pulses. As a result of this the base of T3383 is drawn against ground, the transistor starts to conduct and the output stages are blocked via diodes D3356, D3336 and D3316.

A similar protection circuit becomes operative when the output stage and hence the line deflection become defective during operation. To avoid that the charge of the high voltage produces a burn-in point, the colour output stages are cut off by T3383, because C592 cannot be recharged anymore via D591 and D592 starts to conduct.

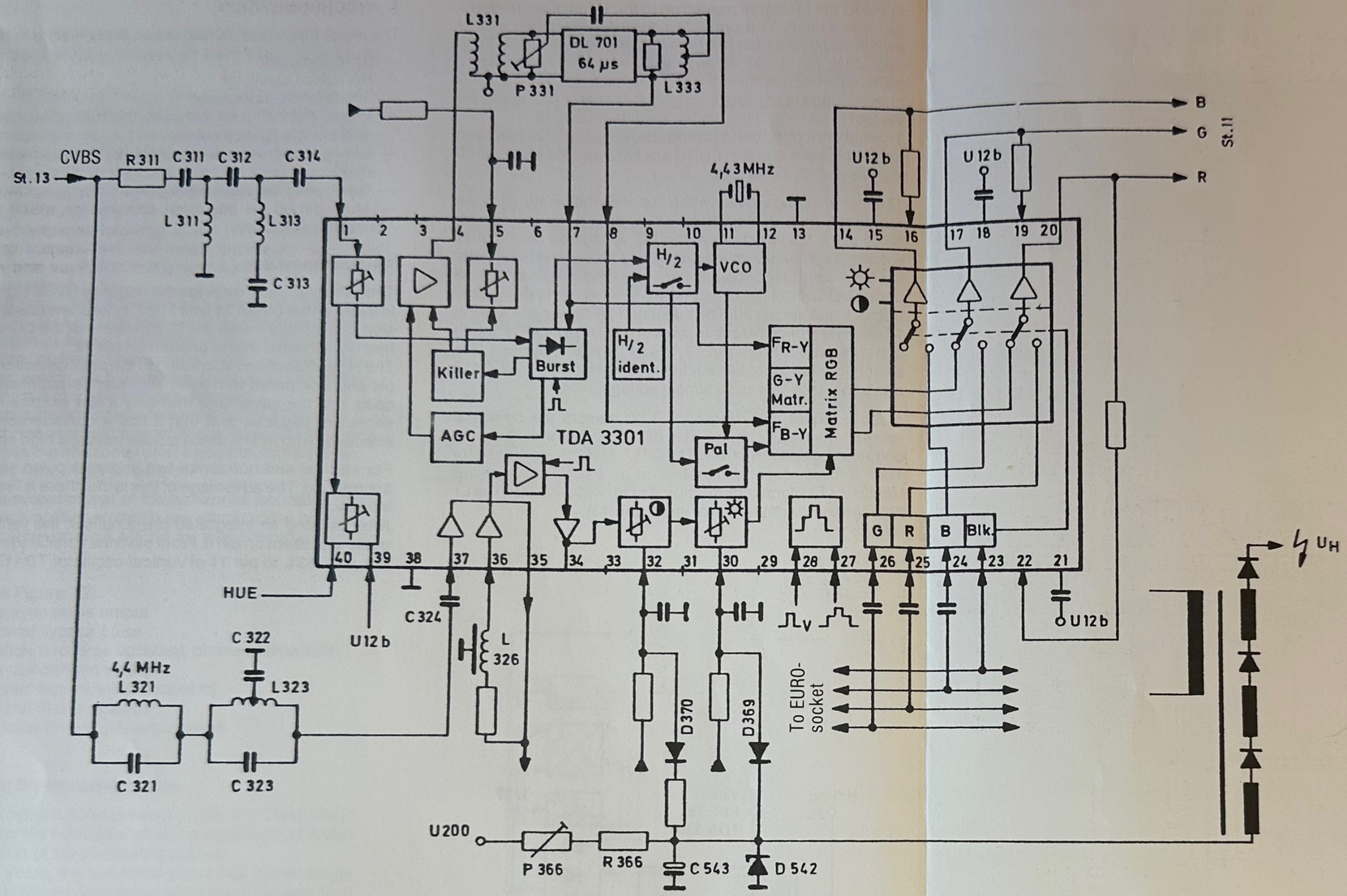


Fig. 4.1

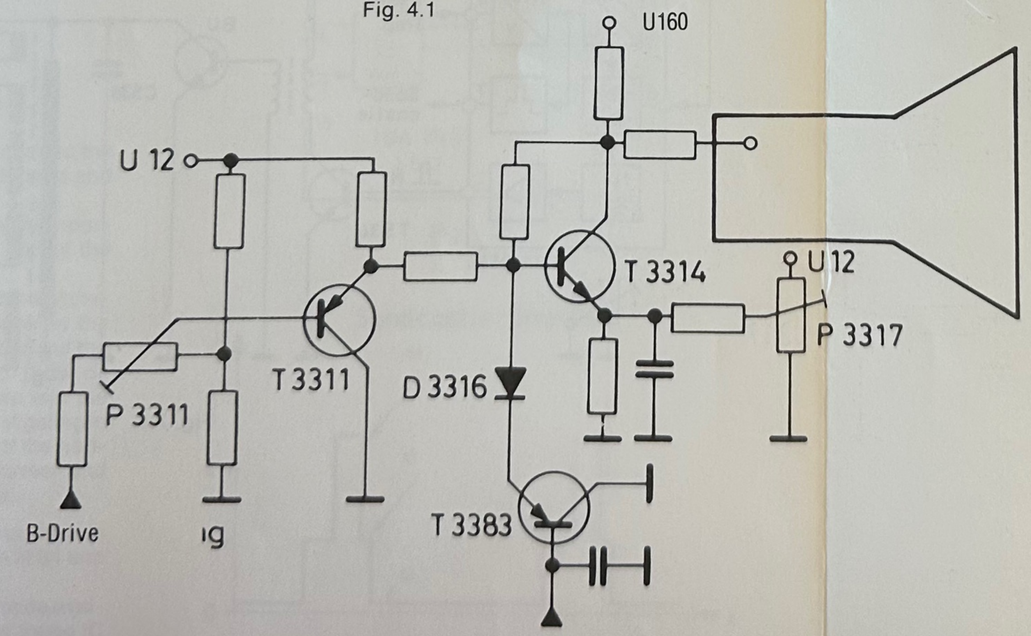


Fig. 5.1 Protection circuit

6. SOUND SECTION

For sound processing use is made of the intercarrier technique.

The integrated circuit TDA4190 takes care of the following functions:

— IF limiter amplifier
— FM demodulator
— Signal source change-over
— Mute circuit
— Tone control
— Volume control
— LF output stage with 4 Watt output power

From the CVBS output of the IF amplifier the IF sound signal is disconnected via C411 (see Fig. 6.1) and ceramic filter K411 and applied to the input, pin 2, of limiter ampifier TDA4190. The FM signal passes through the limiter amplifier and arrives at the FM demodulator. The demodulator circuit between pin 7 and pin 8 has been adjusted for IF sound (max. LF amplitude). After passing an amplifier stage, the LF signal is present on pin 9 and on the LF outputs of the EURO socket, pins 1 and 3.

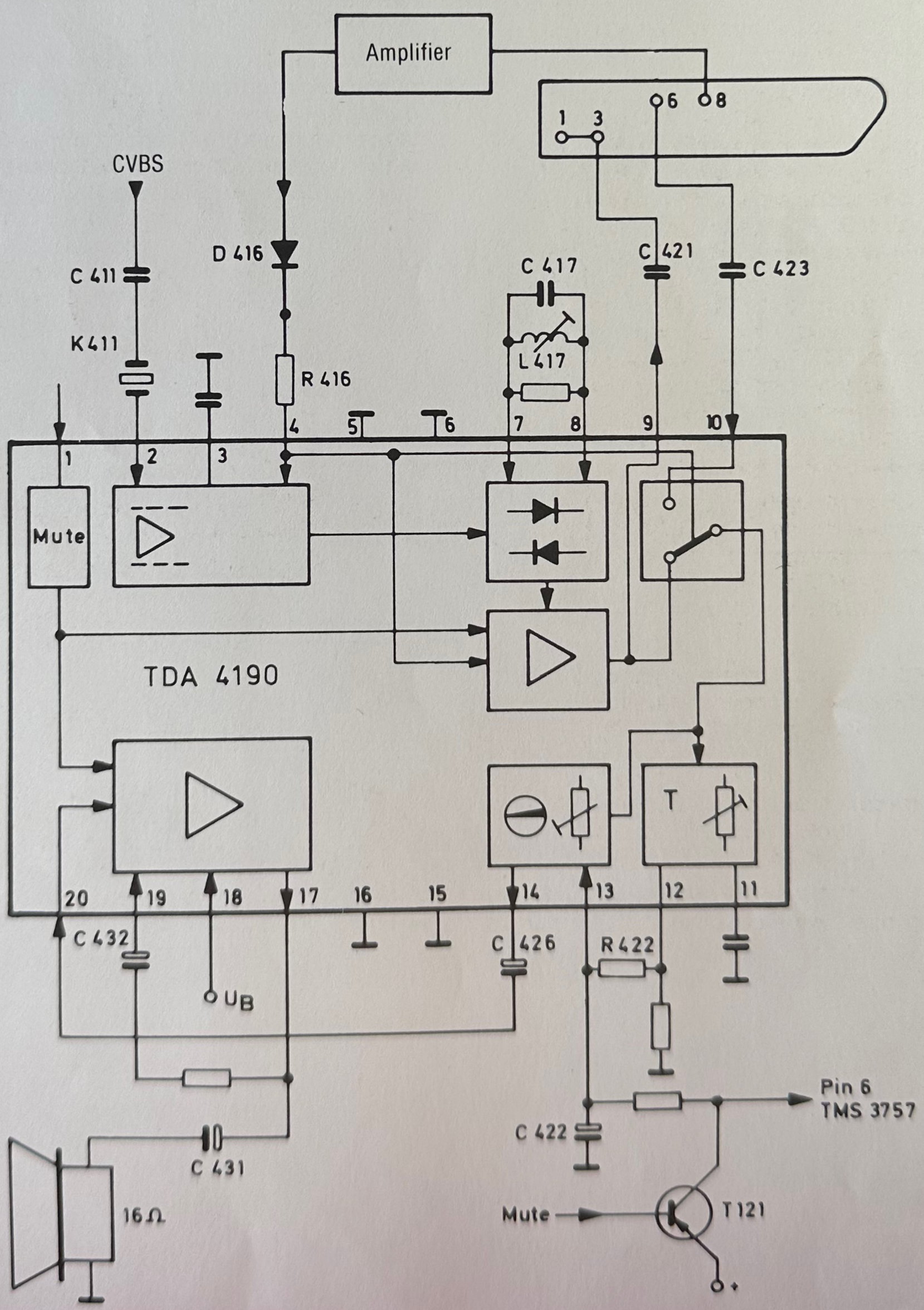


Fig. 6.1

In the IC the LF signal passes on to the signal source change-over switch. The control voltage for the change-over switch is derived from the AV switching voltage. If the TV is operative, pin 4 lies on a L-level, with which the signal switcher switches through the television sound. If a switching voltage is applied, the signal switcher is changed over via D416, R416 and the limiter amplifier is cut off.
This makes it possible to reproduce the sound that has been applied via pin 6 of the EURO socket input for external LF signals pin 10, TDA4190).

The signal change-over switch supplies the LF signal to the regulating units for sound intensity and tone. Volume control takes place via variations in the DC voltage on pin 13 (min. volume 3 V, max. volume 2,4 V). A connection via R 422 with the tone control input takes care of a physiological volume control. On pin 14 the LF signal is branched off to trigger the output stage via pin 20. The maximum LF power of 4 Watt at 16 Ohms is sufficient for this class of sets. An extra IC cooling is not required. From pin 17, the LF signal is applied to a switchable loudspeaker socket and loudspeaker via C432 and L431. U27 serves as supply voltage.

A mute circuit with transistor T121 rejects the sound at search tuning and change-over of the programme: the mute command of pin 16 of the TMS3757 ANL drives transistor T067 into conduction. The L-level on the collector drives transistor T121 into conduction via D077 and cuts off the LF path via the volume control input (pin 13).

7. SYNCHRONISATION

The integrated circuit TDA2594 has the following functions:

— Sync separator
— Horizontal oscillator
— Interference suppressor
— Phase discriminator between the horizontal oscillator and the line flyback pulse
— Change-over of the time constant if the videorecorder is used.
— Generating the sandcastle pulse.
— Mute circuit for television transmitters which do not meet the standard.

7.1 Sync separator

The sync separator receives the negative CVBS signal via a low-pass filter on pin 11 (see Fig. 7.1). Interference suppression takes place inside the IC by means of the DC voltage-free CVBS signal that is present on pin 12.
The circuit functions according to the peak detection principle and, compared with other interference-suppression circuits, has the advantage that only a few external components are required and that it has a considerably higher effectivity with interference pulses having a high amplitude.

For vertical and horizontal two separate pulse separators are applied. The advantage of this is that there is less mutual influence.
After passing an integrated pre-amplifier, the vertical sync pulse is present on pin 8. From pin 8 the vertical sync pulse is fed, via R531, to pin 11 of vertical oscillator TDA1770 S.

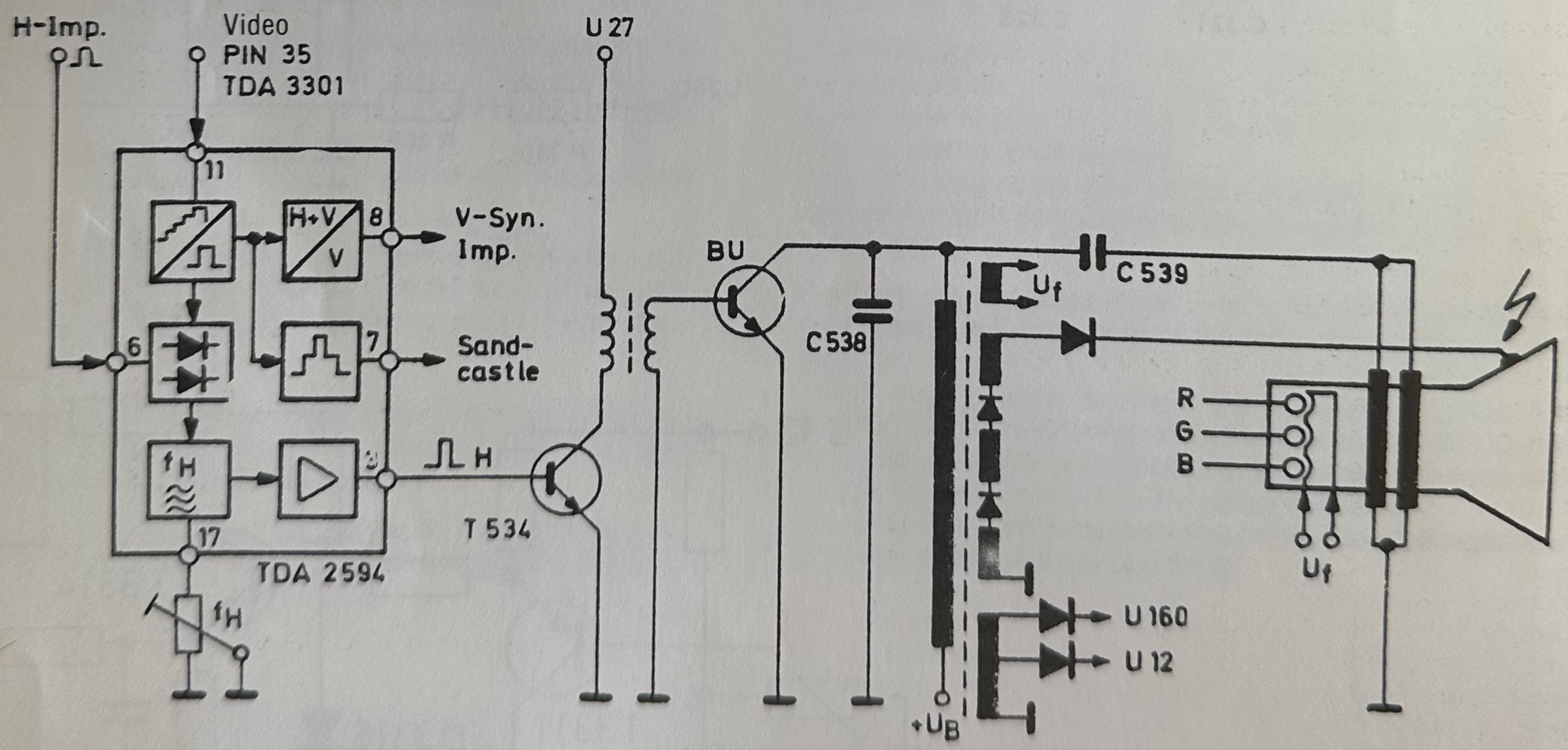


Fig. 7.1

7.2 Horizontal oscillator

For the horizontal phase comparison a positive horizontal flyback pulse of 160 V_{pp} is supplied, via resistor R527, to pin 6 of the IC.

The voltage obtained as a result of the comparison between synchronisation and reference pulses by the phase discriminator is available on pin 15 and is fed back to pin 17 of the IC via R522. On pin 17 the free-running frequency of the horizontal oscillator can be adjusted by means of P521 provided that test point 5a is simultaneously shorted against ground.

The phase-comparison voltage of pin 15 is added to the free-running voltage that has been decreased by U12 through division via P521. In this way a stable synchronisation is guaranteed.

Furthermore the IC was provided with a capture range extension that, in case of large frequency deviations between synchronisation pulse and oscillator, first realizes a rough approximation of both frequencies. With an electronic change-over switch the final phase correction then takes place with the aid of a coincidence detector.

The time constant of the phase comparison, if a VCR or AV is used, is switched over with a switching voltage of + 12 V on pin 13, whereas the horizontal phase position can be changed with P526 over a very large area.

In the IC, the output signal of the horizontal oscillator first drives a pulse amplifier so that a low-ohmic drive pulse of 10 V_{pp} is available on pin 3, MP 5d, for the horizontal output stage.

TDA2594 (see Figure 7.2)
Pin 8 Frame sync pulse output
Pin 6 Horizontal flyback pulse
Pin 13 AV switch-over time constant, phase comparison
Pin 15 Phase comparison voltage
Pin 17 Horizontal free-running frequency
Pin 5 Horizontal phase position
Pin 3 Drive pulse horizontal output stage.

7.3 Generating the sandcastle pulse

The horizontal flyback pulse present on pin 6 of TDA2594 is not only used for the horizontal phase comparison, but also for the generation of the sandcastle pulses.

In the last few years, this universal pulse has increasingly been included in the circuit designs because of the practical advantages it has.

The sandcastle pulse fulfills the following tasks:

— Video-peak white level
— vertical blanking
— horizontal blanking and black-level clamping
— burst gating pulse.

By means of the synchronised horizontal oscillator and the horizontal flyback pulse the sandcastle pulse is formed and applied to pin 7 of TDA2594.

The DC voltage levels of the separate stages are very important for the function of the colour IC TDA3301 and of the colour output stages.

For example, the level a) (in Fig. 7.3) determines the white-level of the colour output stages. Level c) determines the black-level clamping level with + 155 V and carries out the horizontal blanking. Burst gating takes place with pulse d). Once this gating pulse has been coupled in phase with the horizontal oscillator, it is possible to reach the burst gating in proper phase without phase errors (for example of the horizontal output stage or of the line output transformer and horizontal phase regulator P 526) influencing this.

The level informations "a","c" and "d", which are present in the sandcastle pulse, are generated in the IC TDA2594 and are line-frequent.

The level used for horizontal blanking is directly made available on pin 28 of colour IC TDA3301 by pin 1 of frame IC TDA1770.

7.4 The muting circuit

In the IC the frame and line sync pulses drive a TV identification stage which supplies a mute voltage of 11,5 V to pin 9 in case of a correct television signal and a mute voltage of approx. 0,1 V in case there is no television signal or a television signal that does not comply with the standards.

If there is a signal that does not meet the standards, the mute information switches the LF signal path off via diode D121 and transistor T121; at the same time, the mute voltage serves as transmitter identification on pin 13 via diode D013.

7.5 Generating the operating voltage

The standby mode voltage U12, which is obtained from the negative-going line pulse in the line output stage through forward stroke rectification if the apparatus is on, is lacking.

During this time, the operating voltage for the line IC, is derived from voltage U27 via resistor R503 on pins 1 and 2 of the IC, and thus guarantees free oscillation of the horizontal oscillator. The signal path to the line output stage has been shorted to ground via the collector emitter trajectory of transistor T583.

After a switch-on command (on/off) the transistor is cut off, the line output stage is operative and the + 12 V voltage is available via diode D504 for the line IC.

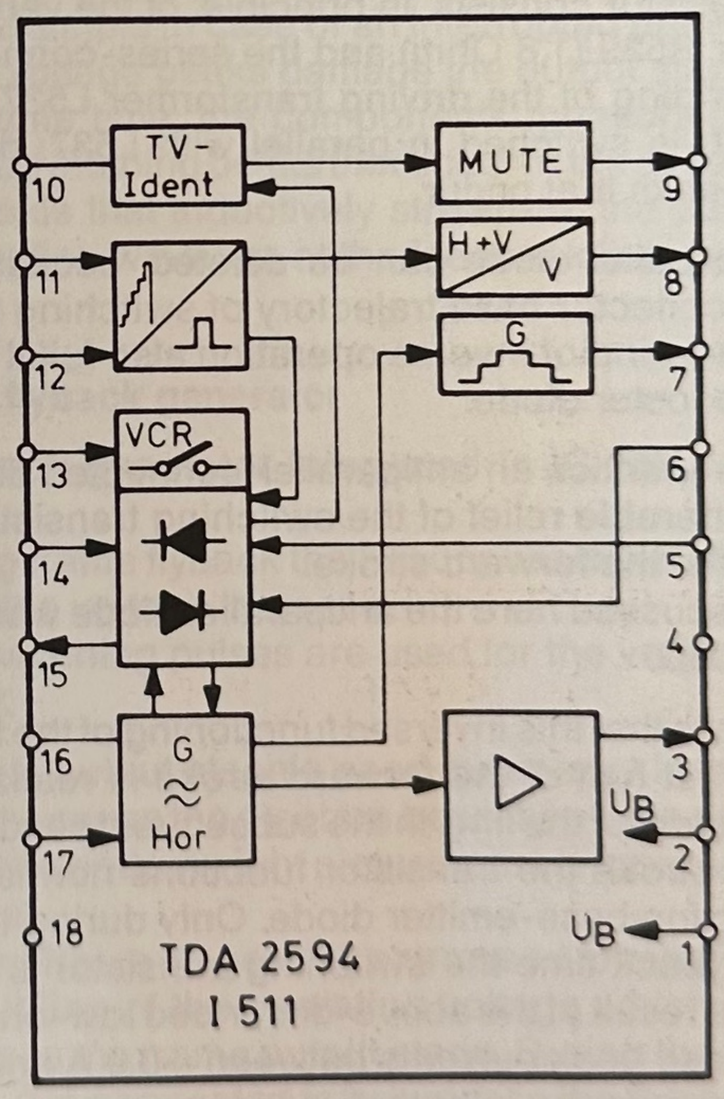


Fig. 7.2

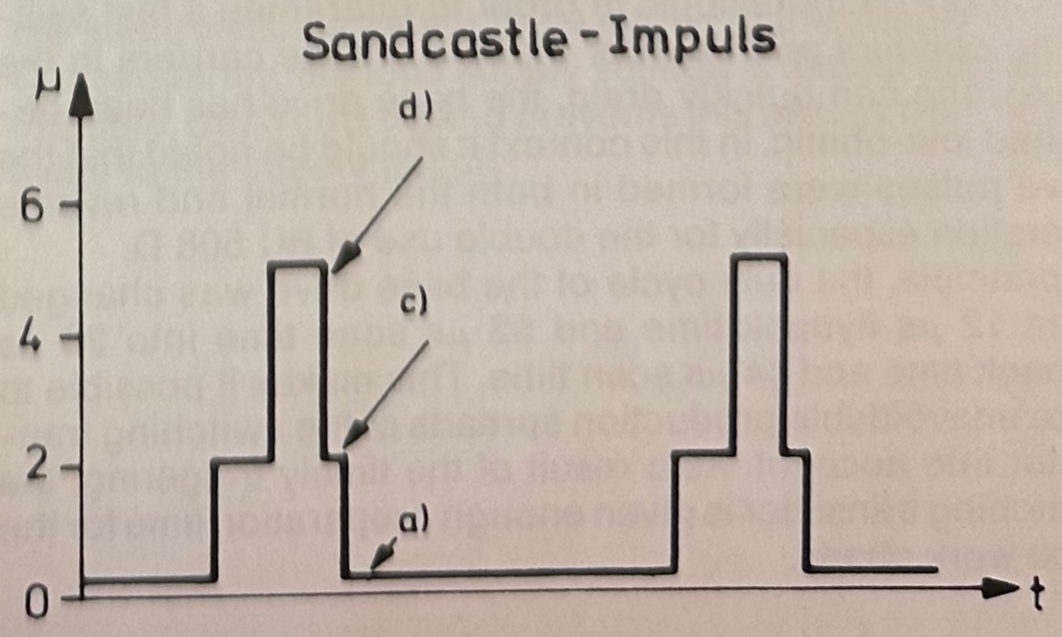


Fig. 7.3

8. THE LINE OUTPUT STAGE

8.1 The horizontal driver stage

The horizontal output stage of TDA2594 supplies, on pin 3, line-frequent drive pulses for driver stage T534 (see Fig. 8.1). From the wiring of driver transistor BC637 it can be seen that it is a very low-ohmic current source driving, which, via a driver transformer, supplies the line sampling pulses to the horizontal output stage.
In parallel with the primary winding is an RC network which, during the cutoff phase, limits the high voltage peaks on the collector of transistor T534. The transformation ratio is 7 : 1, at which ratio base control currents of up to 0,9 A peak can be attained on output stage T539.
Both stages work alternately with respect to one another, i.e., when T534 is cut off, T539 is driven into conduction and vice versa.
The circuits of both transistors were designed for fast switching behaviour and slow switching dissipation.

Transistor T583, which is situated off the base T534 with its collector-emitter trajectory, realizes the stand-by operation. In this case the μP (pin 29) supplies an H-level, T583 starts to conduct and, consequently cuts off the triggering of horizontal driver stage T534. Because of this measure, the line output stage cannot work either, so that the switched mode power supply comes into the standby mode.

8.2 The horizontal output stage

As we have seen in the preceding section, the horizontal output stage - horizontal switching transistor would be more correct - is alternately controlled according to the switched-mode principle.
The base resistor consists, in principle, of the very low-ohmic resistor R539 (1,8 Ohm) and the series-connected secondary winding of the driving transformer L537. Resistor R539, which is switched in parallel with L537, damps the switching peaks that occur.

The extra parallel diode can be deleted, because in this design the collector base trajectory of switching transistor T539 can in a kind of inverse operation also fulfill the function of the booster diode.

However, in practice an antiparallel-connected diode causes a considerable relief of the switching transistor during the first half of the forward stroke.
In the set discussed here the antiparallel diode was integrated in BU 508D.

Fig. 8.2. shows that this inversed functioning of the transistor during the first half of the forward stroke is realized up to about the middle of the line. In the subsequent second half of the forward stroke the transistor functions normally again with conducting base-emitter diode. Only during the relatively short flyback time the switching transistor is not conducting. As a result of the above-described low-ohmic base wiring the base peak currents between +0,9 A and —0,9 A can quickly flow away in both directions.

It is imaginable that the still higher emitter currents (IE max. = 4,5 A) cause enormous "floods" of charge carriers in the N-P and P-N transitions. In order to guarantee a fast switching conduct and in order that the charge carriers in the base zone can quickly drain, the base drive has been designed low-ohmic. In this context it should be noted that the drive pulses were formed in both the normal and reverse operation especially for the double use of BU 508 D.
In principle, the duty cycle of the base drive was changed from 12 μs flyback time and 52 μs scan time into 20 μs flyback time and 44 μs scan time. This makes it possible to take unavoidable production spreads of the switching transistor into account. As a result of the timely triggering, the switching transistor is given enough preparation time for the next work phase.

The supply voltage of the horizontal output stage is taken from the switched-mode power supply circuit and is 27 V$_{\overline{\ldots}}$
After this the precise drive and switching rhythm during one line period is described. The following explanations of the function of the line output stage are based on the principle of the switched resonance circuit. Thereby the line switching transistor functions through its three operating conditions: conducting, reverse conducting and cutoff, in such a way that the charging and discharging processes of the collector capacitances and inductances provide for the precise scan and flyback intervals. The description of the work phases is started in the middle of the line. This time is called "t1".

At t2 (see Figs, 8.3 and 8.4) the driver transistor cuts off, the line switch conducts (closed). In switched-on condition, C539 is still charged from the previous cycle. This capacitor now functions as booster capacitor and, through the beginning discharging process, causes the deflection current to flow through deflection coil LA via switching transistor T539.

In the same time the primary induction of high-voltage transformer LT1 is connected, via the switching transistor, to the supply voltage. The resultant current I-LTr is added to the deflection current I-LA in the line switch. Both currents form magnetic energy in the coils through which they flow.

Already before the end of the second half of the forward stroke the driver transistor is driven into conduction again (see Fig. 8.5 and Fig. 8.6).Thus it is guaranteed that in the switching transistor the charge carriers resulting from the high collector emitter current are timely derived at t2.

Because of the timely cutoff of the switching transistor, the horizontal flyback can start at t2.

The current direction in LTr and LA do not change in the beginning. Both currents quickly charge the line resonance circuit capacitor C538 up to the peak flyback voltage of 900 V (time t3).

When t3 is reached, the charging process of C538 has ended, I-LA and I-LTr go to zero and reverse polarity at t4. The current reversal is caused by capacitor C538 which has now discharged via LA LTr (see Fig. 8.7 and 8.8).

The relatively short flyblack time of approx. 14 μs can be explained by the high charging current I-LA and I-LTr in C538 with a capacitance of approx. 30nF.

Immediately after t4 the resonance circuit has a natural inclination to oscillate back.
The beginning hereof can be seen in diagram U_{CE}/BU 508 immediately after t4 (see Fig. 8.9 and 8.10).

The inclination of the line resonance circuit to continue oscillating would form the negative half wave on collector T639.
After reaching the threshold voltage of the antiparallel diode: collector mass in the housing of T 539 of approx. — 0,7 V this trajectory starts to conduct. The anti-parallel diode acts as booster diode between t4 and t1.

At t1 the magnetic energy has been built down, the deflection current and the current in the high-voltage transformer change polarity in the middle of the line, C539 has been charged. The process starts again.

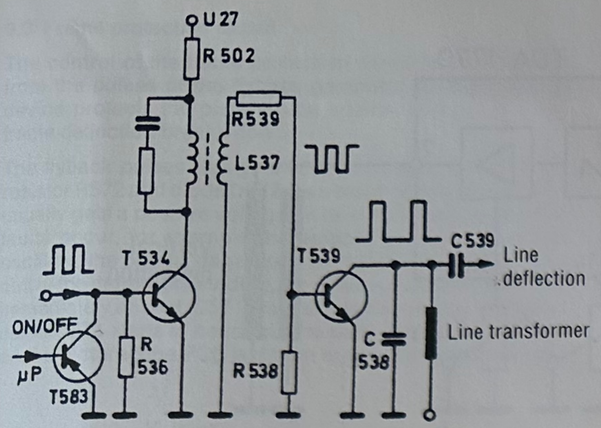


Fig. 8.1

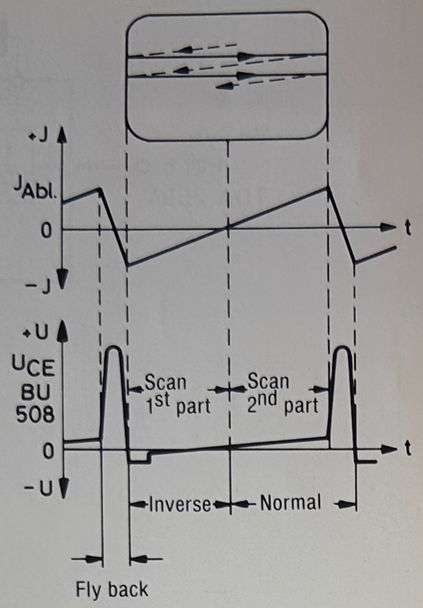


Fig. 8.2

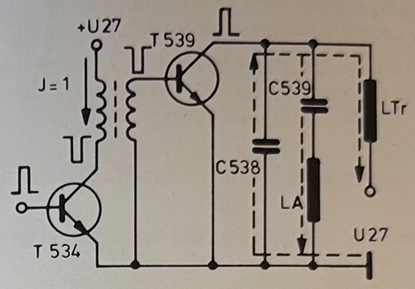


Fig. 8.7

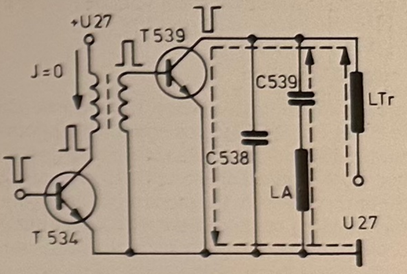


Fig. 8.9

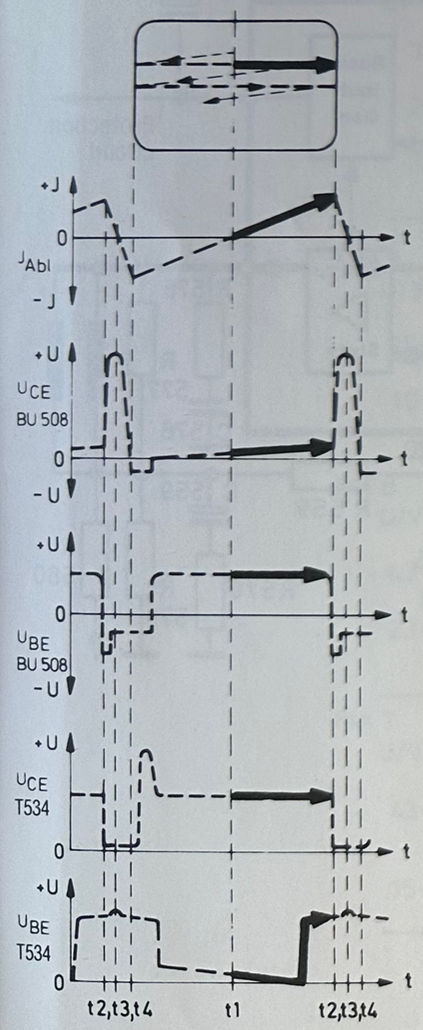


Fig. 8.4

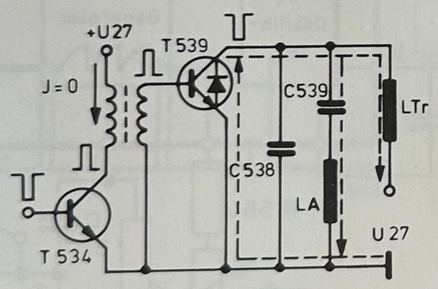


Fig. 8.3

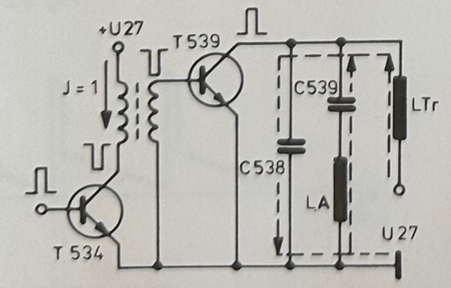


Fig. 8.5

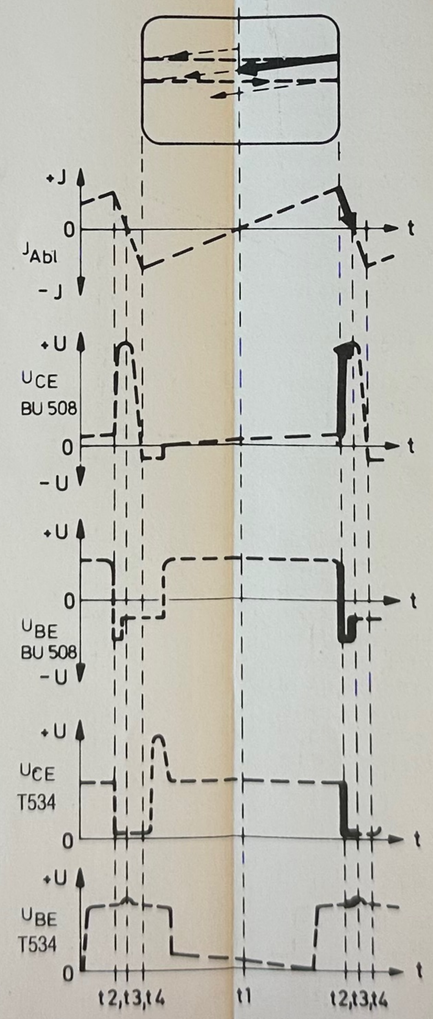


Fig. 8.6

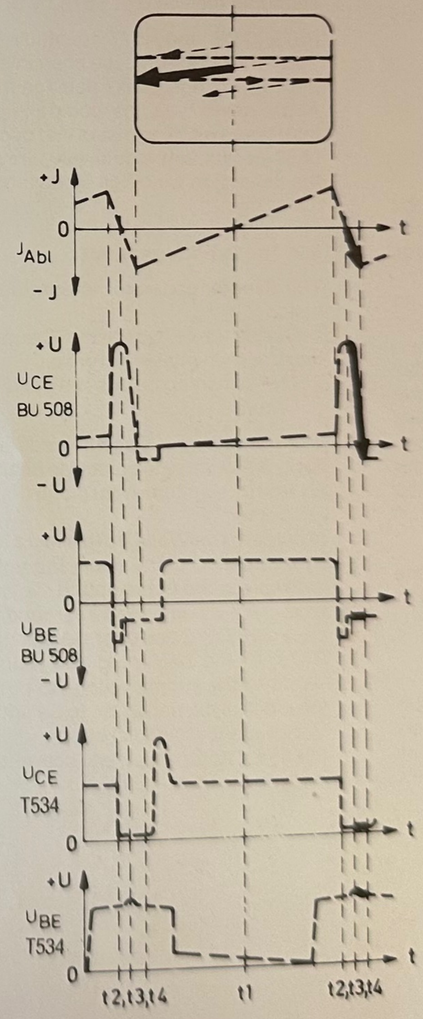


Fig. 8.8

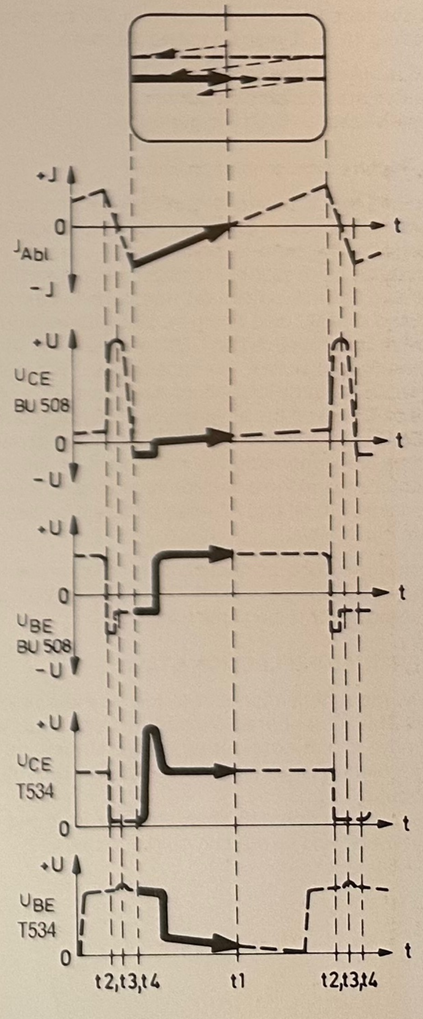


Fig. 8.10

8.3 Generating high voltage

The high-tension transformer also contains the cascade. The secondary winding of the line output transformer was divided into three parts and the high-tension rectifier diodes are connected between the separate winding parts. This way of increasing the high tension can be realized without using the heavily loaded capacitors used so far. On the one hand, this increases the reliability and, on the other, it is a space-saving, compact solution.

The resistance divider as well as the potentiometers of the Ug2 and the focus adjustment have mechanically been integrated in the transformer. The auxiliary winding with connections 6 and 8 supplies the heater voltage for the picture tube.

8.4 Beam current limitation

The base capacitor of high-tension transformer C543 is charged via P366, R366, R369 (see complete diagram). The parallel-situated Zener diode D542 acts as charge limiter for the capacitor. Both diodes D369 and D370 are usually cut-off by the charging voltage of the electrolytic capacitor. As a result of an increasing beam current, C543 is continuously discharged, causing the charge to decrease such that D369 starts to conduct and the brightness adjusting voltage decreases. If this should not be sufficient, the contrast adjustment voltage is adjusted via D370.

8.5 The secondary supply voltage

The supply voltage U160 for the colour output stages on the picture tube PCB is obtained from the secondary auxiliary winding 10 to 12 (see complete diagram).

U16 is obtained by rectification of the negative flyback pulses that are available on connection 7.
By stabilizing U16, U12 is generated.

8.6 Picture tube protection circuit

To avoid that, in case of defective deflection, the picture tube capacitance, which is still charged with high tension, discharges via a burn-in point via the system, a protection circuit has been realized for both vertical and horizontal.
The line flyback pulses on transformer connection 7 are rectified in D591 and charge C592. The voltage on the cathode of D592 is such that D592 is usually cut off. If there are no line flyback pulses, the capacitor is discharged via R592 so that D592 starts to conduct. As a result of this process, the base of T3383 on the picture tube PCB has ground potential via D592 and R592. The PNP transistor is driven into conduction and connects the transistors of the three colour output stages at the base side to ground. Consequently, the transistors cut off and a further picture tube beam current is made impossible.

The picture tube protection circuit for breakdown of the frame deflection works with D572, C571, R571 and D571 in the same way on the same transistor.

9 VERTICAL DEFLECTION STAGE

The vertical deflection is realized by the one-chip-IC TDA 1770. This IC is characterized by little external wiring. Furthermore it has no external output stages, as the IC can trigger picture tubes up to 20" direct with deflection currents of about 0,9 V_{pp}.
The power supply (16 V) is realized from the line output transformer, just as the line output stage.

The functions of TDA1770 are (see Fig. 9.1):

- Vertical oscillator
- Saw-tooth generator
- Output stage for direct triggering of the deflection coils
- Flyback generator
- Frame blanking
- Frame protection circuit

9.1 Saw-tooth generator and output stage

Frame IC TDA1770 receives the frame sync pulses, which are supplied by the sync IC, on pin 11 (see figs. 9.2 and 9.3). After passing through an internal sync stage, the pulses trigger the frame oscillator. A linear saw-tooth having an extremely constant frequency is available on pin 9.

In the IC, the frame oscillator drives the saw-tooth generator whose operating voltage is adjusted via series resistor R564 and picture amplitude control P564.

Linearity correction takes place in the negative feedback branch between pin 18 and pin 17. P566 is the linearity control.

After the internal amplification, the output signal for the deflection coils is available on pin 7.
The deflection current is max. 0,9 A_{pp}. In order to guarantee good linearity, part of the output signal is via resistor R559 led back in opposite phase to the input of the output stage.

The vertical picture centring is effected with resistor R579. In case of service, for example after replacement of the picture tube, a correct vertical picture centring can be obtained by changing the value of R579 by +/_ of a standard value.

R576, C576 and R577 constitute the basic load and avoid that, for example in case of an interrupted deflection circuit, too high voltage peaks damage the output stage.
At the same time, the components mentioned reduce the inductive switching peaks that occur in the deflection circuit. L582 avoids that inductively strewn-in line parts arrive via the deflection windings at the feedback input, pin 20, of the IC.

9.2 The flyback generator

The flyback generator integrated in IC TDA1770 has two tasks:
1 During frame flyback the IC supplies the switching voltage for the voltage increase.
2 The switching pulses are used for the vertical protection circuit.

The frame output stage's need for energy is largest during flyback, because the electron beam has to be supplied quickly from the bottom-right picture-screen corner to the upper left corner.
In modern frame stages this extra need for energy is realized by a doubling of the operating voltage which is only made available to the frame output stage. During the frame sweep time, pin 3 is connected to ground via the flyback generator, capacitor C572 can charge itself up to the supply voltage via D573. At the beginning of flyback, the flyback generator switches the supply voltage to pin 3, causing the charge of the electrolytic capacitor to be added to the supply voltage. Consequently, the total supply voltage is almost doubled. At this time, D573 cuts off and prevents this energy from flowing away to the supply circuit.

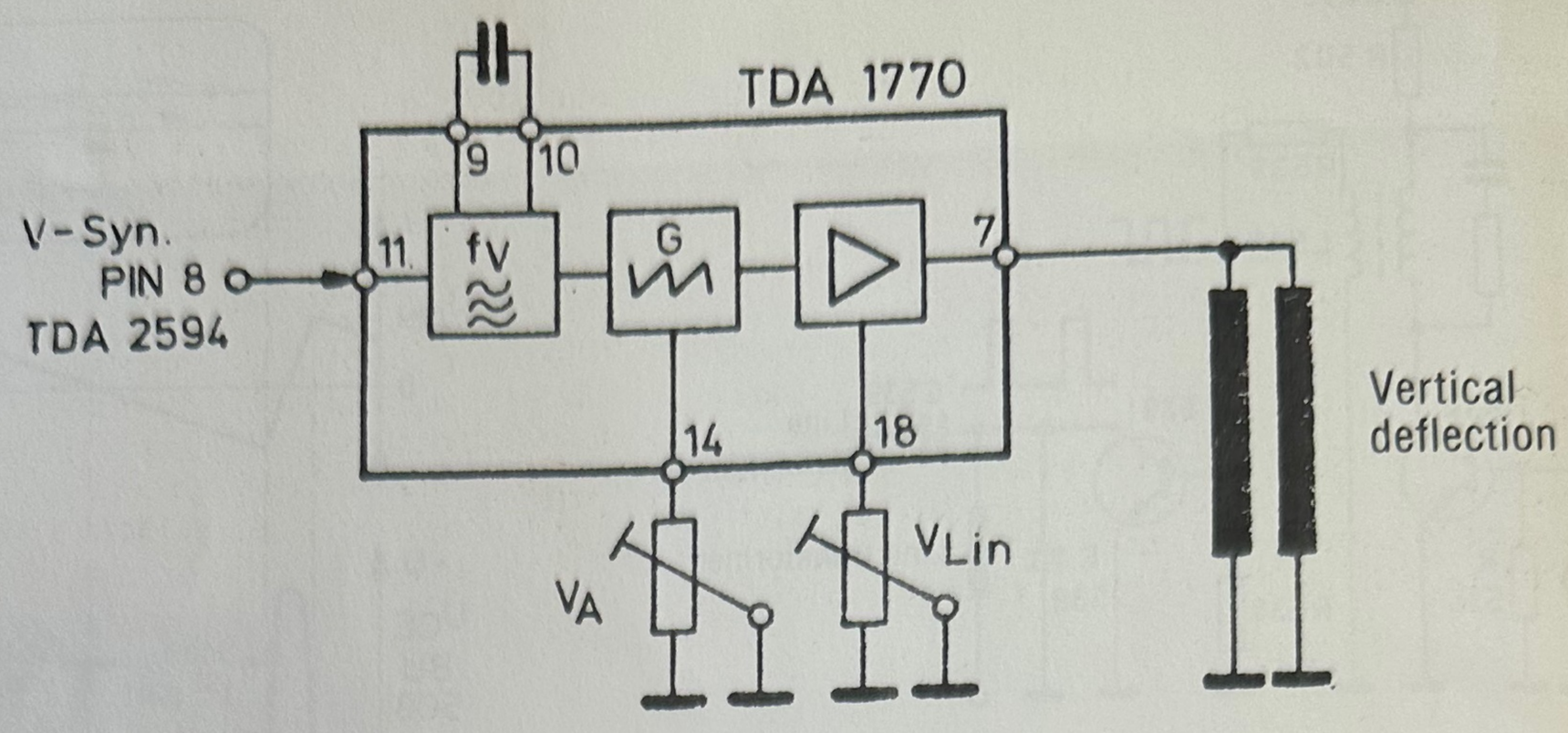

TDA 1770
9
10
11
fV
G
7
V-Syn.
PIN 8
TDA 2594
14
18
VA
VLin
Vertical
deflection

Fig. 9.1

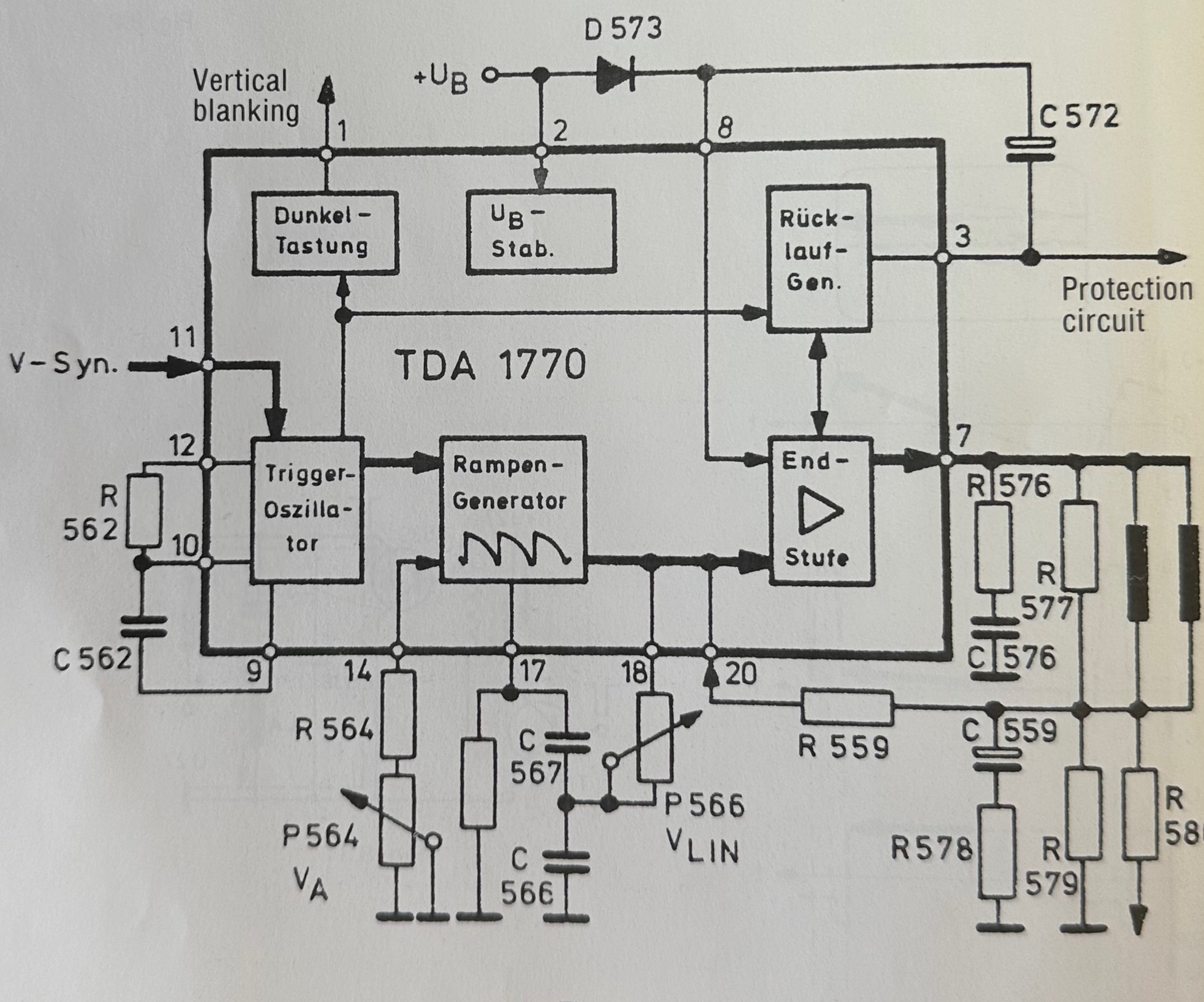

D 573
+UB
Vertical
blanking
1
2
8
C 572
Dunkel-
Tastung
UB-
Stab.
Rück-
lauf-
Gen.
3
Protection
circuit
11
V-Syn.
TDA 1770
12
R
562
10
Trigger-
Oszilla-
tor
Rampen-
Generator
End-
Stufe
7
R 576
R
577
C 576
C 562
9
14
17
18
20
R 564
C
567
P564
VA
C
566
P566
VLIN
R 559
C 559
R578
R
579
R
580

Fig. 9.2

9.3 Frame protection circuit

The control of the frame protection circuit is also derived from the pulses of the flyback generator. This protection device protects the picture tube against burning in if the frame deflection breaks down.

The flyback pulses charge electrolytic capacitor C571 via resistor R572 and diode D572. As a result of this, diode D571 usually gets a positive voltage on its cathode and cuts off. If faults occur, for example the vertical oscillator does not oscillate, the output stage does not function or a short-circuit in the deflection winding, the flyback pulses on pin 3 are immediately absent. C571 discharges via resistor R571 and diode D571 starts to conduct. The base of transistor R3383 on the picture tube PCB is drawn to ground by the low-ohmic diode trajectory, the transistor switches through, brings the bases of the three colour output stages to ground potential via the collector-emitter trajectory and thus succeeds in cutting off the picture tube.

9.4 The frame blanking pulse

The frame blanking is generated from the information of the frame oscillator and the flyback generator. The frame blanking pulse is coupled out on pin 1 of the frame IC. Then the pulse is limited to 10 V_{pp} by Zener diode D574 and presented, via resistor R 356, to colour IC TD3301 on pin 28 for further processing .

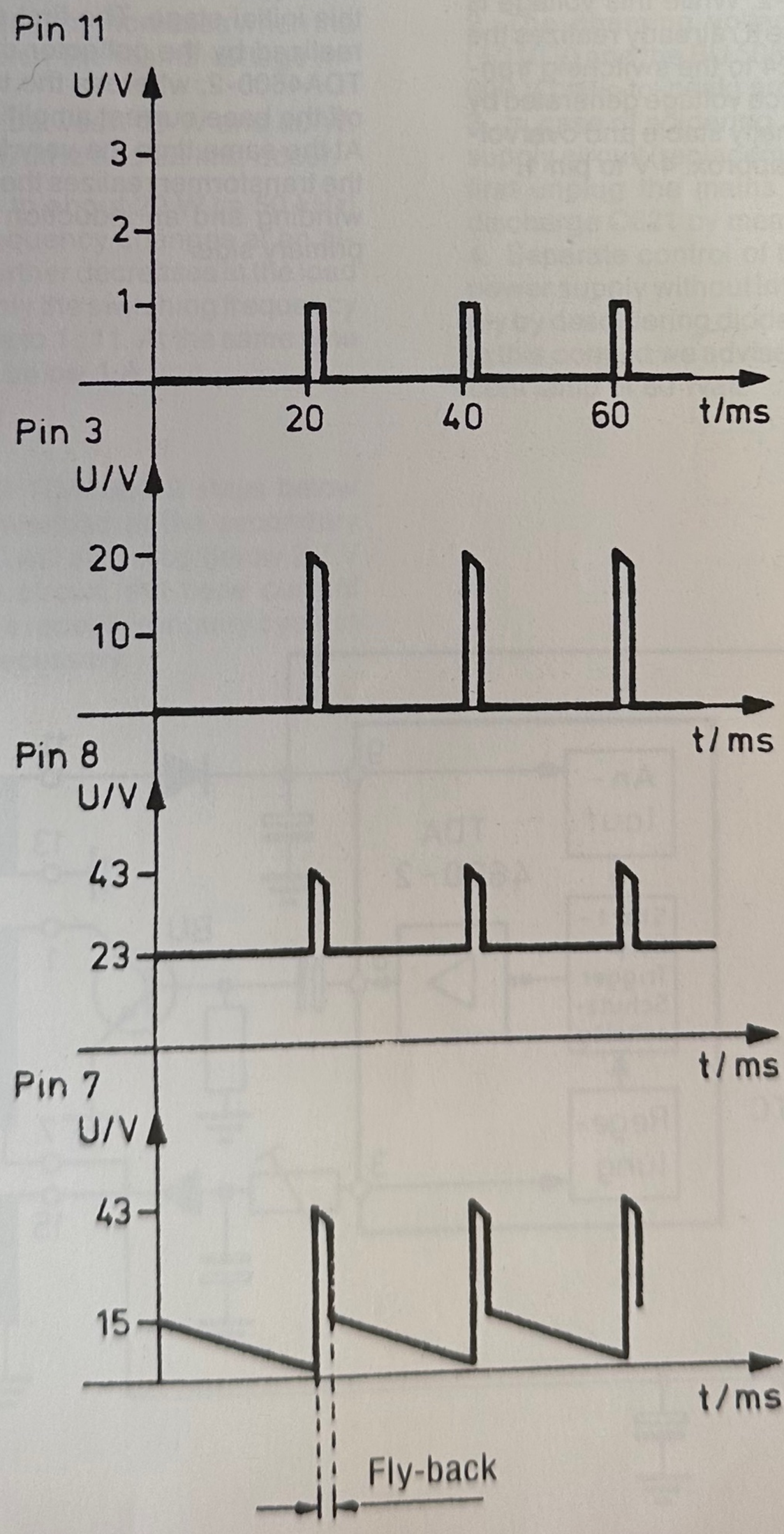


Fig. 9.3

10 POWER SUPPLY

10.1 Introduction

For stabilization, control, starting and protection circuit, this apparatus uses an IC: TDA4600-2 (see Fig. 10.1). The power switching stage is built around the BU508. The, switched mode transformer realizes the main separation between the primary and secondary winding.

The stabilized operating voltages U110, U27, U8 and U5 are available on the secondary side. The remaining supply voltages U200/U160, U23 and U12 are obtained from the line flyback voltages.

The AC mains voltage arrives at the degaussing coil via the mains switch and the mains suppression filter and at the bridge rectifier D613 via the switch-on current limiter R611. An operating voltage of approx. 310 V is quickly formed on charging capacitor C621. Via winding 7-1 of the transformer this voltage is also available as voltage on the collector of switching transistor T623 (see complete diagram).

As, at this moment, there is not yet a base drive voltage available for BU508, initially the voltage is not loaded.

10.2 Starting behaviour

The switched mode power supply is started with a separate starting circuit. R611 supplies a starting voltage to C626 via the PTC, R629 and R628. The charge of C626 forms on pin 9 the supply voltage for IC TDA4600-2. While this voltage is building up, the voltage control in the IC already realizes the charging of coupling capacitor C624 to the switching transistor. On the other hand, the reference voltage generated by the voltage control supplies a thermally stable and overvoltage-resistant reference voltage of approx. 4 V to pin 1.

This reference voltage constitutes the operating voltage for all other IC stages, with the exception of the control logic, but does not become operative initially. When 12 V on pin 9 are reached, the reference voltage is suddenly released and, via a further stabilization, the power supply of the control logic is switched on.

The starting delay described is necessary to attain a sufficiently high charge in C624 and hence a safe start of switching transistor BU508. After the start of the power supply, the supply voltage for the IC is obtained from connection 11-13 of the transformer.
Approx. 20 V are available as a result of rectification on C626 and charging in C626.
Consequently, the start circuit does not become operative via R628 and R629.

10.3 Operation

The starting pulse drives switching transistor T623, BU508 into conduction for the first time. This results in a current via the collector emitter trajectory and transformer winding 1 - 7. This increasing current causes a magnetic field which drives the transformer close to magnetic saturation. During this process magnetic energy is stored.

Initially, a controlled adjusting function is not yet possible in this initial stage. The first switch-off of the BU therefore is realized by the collector current imitation circuit on pin 4, TDA4600-2, whereas the trigger holding flip-flop switches off the base current amplifier.
At the same time the very fast decreasing magnetic field in the transformer realizes the energy transfer in the secondary winding and an induction in the auxiliary winding on the primary side.

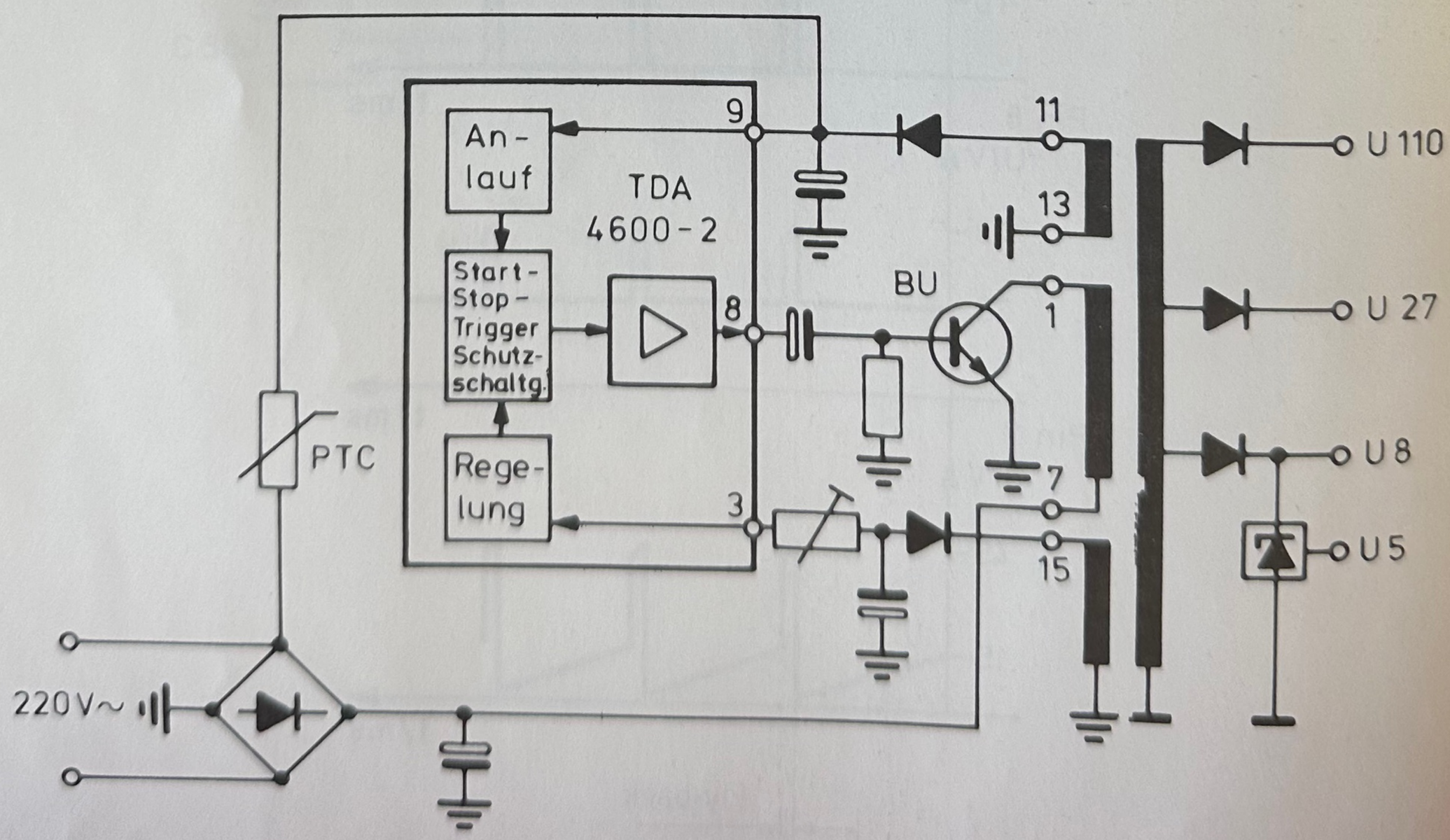


Fig. 10.1

On pin 2 of TDA4600-2 the zero crossings of the pulses supplied by connection 15 of the feedback coil are registered and passed on the control logic.
The pulses coming from the same source, rectified in D636, serve on pin 3 of the IC as output quantity and a overload and stand-by identification. The AGC amplifier operates on an input voltage of approx. 2 V, which is influenced by potentiometer P636. The control voltage on pin 3 and the collector current imitation voltage on pin 4 and the reference voltage on pin 1 take care of the overload identification and limit in such cases the control range of the AGC amplifier. Capacitor C627 determines the largest possible collector current of the switching transistor and thus fixes the desired control range.

In the trigger flip-flop the output levels of the AGC amplifier, the collector current imitation circuit and the overload identification circuit are compared and passed on to the control logic. The control logic fixes, dependent upon the start circuit and the zero crossing identification, the control of the base current amplifier and of the base current circuit, respectively.
A current feedback has been realized with R631 between pin 8 and pin 7. This current feedback determines the maximum amplitude of the base drive current for the BU.

Dependent upon the secondary load, the control information of connection 15 of the transformer will lower and, via the control circuit, reach stabilization through a slower switching frequency, in accordance with a longer operating current.
And conversely the switching frequency increases when the secondary load decreases or when the mains voltage increases.
Thus it is possible that, at loads between 40 W and 80 W, switching frequencies between 37 kHz and 22 kHz occur.

If the secondary load decreases to about 20 W (= 50 kHz) practically only the switching frequency changes at an almost constant duty cycle (1 : 3). Further decreases in the load to, for example, 1 W change not only the switching frequency (= 70 kHz), but also the duty cycle to 1 : 11. At the same time the collector peak current drops below 1 A.

10.4 Protection

When the voltage level on pin 9 TDA4600-2 stays below 7,4 V, for example because of overload at the secondary side, the voltage on pin 5 of the IC will also drop below 2,2 V and cuts off, via the protection circuit, the base current amplifier. The IC realizes thereby a repetitive inquiry cycle in order to restart automatically if necessary.

In case of operation without any load at all, the IC, as described in the previous chapter, will increase both the switching frequency and the duty cycle.
In both extreme applications: overload and no load at all, the supply circuit consumes only about 8 Watt from the mains.

10.5 Stand-by

When, in case of a working set, the mains voltage is briefly interrupted, the set adopts the stand-by mode. The set switches on again after a programme key has been depressed. In the stand-by position, pin 29 of the μP IC 11, MC 6805, supplies an H-level to the base of transistor T583. The transistor is thus driven into conduction, its collector emitter trajectory is low-ohmic and avoids control of the line control stage T534. Consequently the line output stage T539 cannot work either and the secondary operating voltages U160, U23, U16 and U12 of the line output transformer are not present.

10.6 Servicing hints

As, in the stand-by mode, the main supply circuit is energized and functions under voltage, the way of servicing as applied so far for the switched mode supply circuits cannot be used anymore!

The following points should be taken into consideration:

1. In the stand-by mode all secondary voltages of the switched mode transformer are present.
2. The charging voltage of electrolytic capacitor C 621 (+310 V) and the BU 508 collector switching pulses (approx. 600 V peak-to-peak) are present also.
3. In case of soldering activities on the primary side of the supply circuit (replacement of the IC or BU 508), we advise to first unplug the mains plug from the wall socket and to discharge C621 by means of a low-ohmic resistance.
4. Separate control of the functions of the switched mode power supply without influences from the chassis, for examply by desoldering diodes D651, D656 and D658, is possible. In this context we advise you to load U110 with an incandescent lamp of 60 Watt.

11. 12-VOLT BATTERY POWER SUPPLY

The task of this circuit (see Fig. 11.1) is to supply the 8 V and 27 V supply voltages from the battery voltages between 10,5 V and 14,5 V. Furthermore this circuit contains the electronic switch-on and switch-off circuit which is needed for the μC controlled control circuit.

11.1 U8 power supply

If the set is switched on, transistor T9632 cuts off. T9637 is driven into conduction via safety resistor R9638, 1 Ohm and R9637. At the same time the collector-emitter trajectory of T9638 (BD 535) also becomes low-ohmic. Dependent upon Zener diode D9637 the emitter of BD 535 supplies an operating voltage that is stabilized at 8 V.

11.2 U27 power supply

For the generation of U27 a DC converter is required. The first half of the voltage comparator IC9601, Pin 5-7 acts as oscillator. Resistor R9604 and capacitor C9603 largely determine the clock frequency of about 20 kHz. This clock frequency arrives as saw-tooth shaped reference voltage at the non-inversing input of the second comparator via series circuit R9616, C9616. On Zener diode D9612 an amplitude stabilization is reached via R9612. The time constant T9613, C9613 mainly serves for a not sudden, but gradual, smooth start of the circuit.

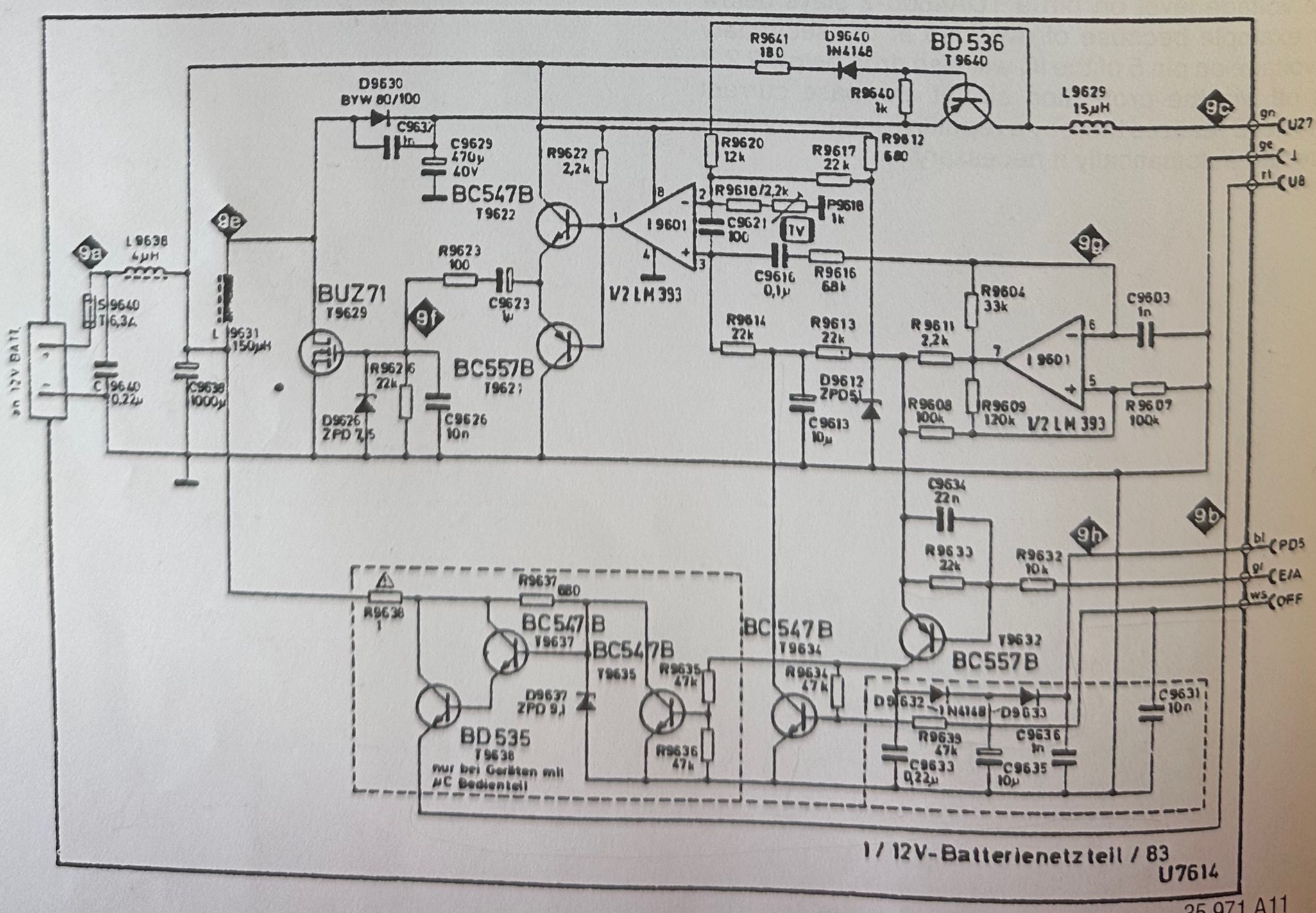
Via voltage divider R9620, R9618 and P9618, the actual value of the main supply voltage U27 is added to the inverting input, pin 2. The main supply voltage can be adjusted for the nominal value by means of the potentiometer. Both transistors, T9621 and T9622, act as a driver stage driving the power switching stage T9629 via C9623.

Via R9623 and Zener diode D9626 with their parallel components, an effective limitation against overvoltages has been installed on the gate of the MOS power transistor. In this way, the maximum permissible drain current can also be kept inside the protected region of operation.

While T9631 is conducting, magnetic energy is being stored in memory coil L9631 (according to the switched-mode principle). At the beginning of the cutoff phase this energy is released very quickly and causes a voltage increase in the coil which can be rectified in D9630 and smoothed out with C9629. With the battery power supply switched on, the Darlington circuit with T9640 causes a low-ohmic switching through of U27; if the converter is switched off, a high-ohmic cut-off.

11.3 Electronic switch-on and switch-off

If the battery power supply is switched off, a L-level is present on the On/off (switch-on and switch-off) input via an auxiliary contact on the mains switch. This causes T9632 to conduct. Transistors T9634 and T9637 also start to conduct. Zener diodes D9612 and D9637 and hence the reference voltages for U8 and U27 are short-circuited, the supply circuits are switched off. In switched-off situation a battery quiescent current of approx. 35 mA flows.



35 971 A11

CS 98 308 GB

Fig. 11.1

12. THE CONTROL SYSTEM

The electronic control system consists principally of two blocks (see Fig. 12):

— microcomputer 6805 K 2 as central processing unit.
— frequency synthesizer with digital-analogue converter TMS3757 ANL.

These two blocks communicate via the I^2C bus and control the control part and the tuning system.
For control of the LED indications, the mute circuits and the band switches of the tuner, extra transistor control stages have been incorporated.

12.1 The microcomputer

Microcomputer MC6805 K2 works as central processing and information unit. This microcomputer has an integrated EE-PROM for the storage of 60 transmitters and 8 analogue values in the memory.

Technical data:

— three 8-bit bidirectional ports
— one 8-bit input port
— 2 k-bytes ROM (software memory)
— 64 bytes RAM space (working store)
— 128 bytes EE-PROM (memory for 60 television programmes and 8 analogue values).

The software of the system, just as the CCIR oscillator frequencies and multiples of 125 kHz are stored in the ROM of the microcomputer which comprises 2 k-bytes. Once again the working store is a RAM with a storage capacity of 64 bytes. Via the input and output ports the control commands are supplied, the LED indications, the frequency synthesizer and the digital-analogue converter controlled.

The local control commands are parallel fed in and composed by an 8×6 matrix with the inputs PD 2 - PD 7 and PA 0 - PA 7. Thus, 48 local control commands are possible.

12.2 Display control and local control scanning

In order to use the in and outputs of the microcomputer for more than one function, the 8 inputs (PA 0 - PA 7) are also used for driving the indication LEDs. Alternately, the keys are scanned and the separate indicator LEDs unblanked. This is done with a frequency of 83 Hz.

Inside a period of 12 ms each programme indication is unblanked for 4 ms (see Fig. 12.2). Scanning of the local control keys is done 500 μs before the end of the 12 ms period.

The programme indication which consists of 7 segments is not only used for programme and channel indication, but also to indicate the adjusted analogue values for sound intensity, brightness, contrast, colour saturation and fine tuning within the 64 possible steps (0 - 63).

The set is switched on via the mains key or, from the stand-by position, by selecting a programme number or via the channel mode or search tuning commands. After a switch-on command has been given, output PB 4 of the microcomputer is still 500 ms high until the output voltage of the switched-mode supply circuit has been built up. During this time, the H-level connects the horizontal control pulses for the line output stage to ground via transistor T583 and thus prevents the line output stage from oscillating too early.

12.3 The tuning system

The frequency synthesizer and digital-to-analogue converter TMS3757 are controlled, via an I^2C bus, by microcomputer MC 6805 K2 and supplies the band switch voltage and the tuning voltage for the tuner already in analogue form. An AFC was not necessary in this system.

The microcomputer communicates the desired channel frequency (CCIR standard frequency) in whole-number multiples of 125 kHz to TMS3757 via the I^2C bus. From the tuner, via the RF divider, the relevant oscillator frequency is available. Both frequencies are now compared and the tuning voltage is adjusted until there is agreement.

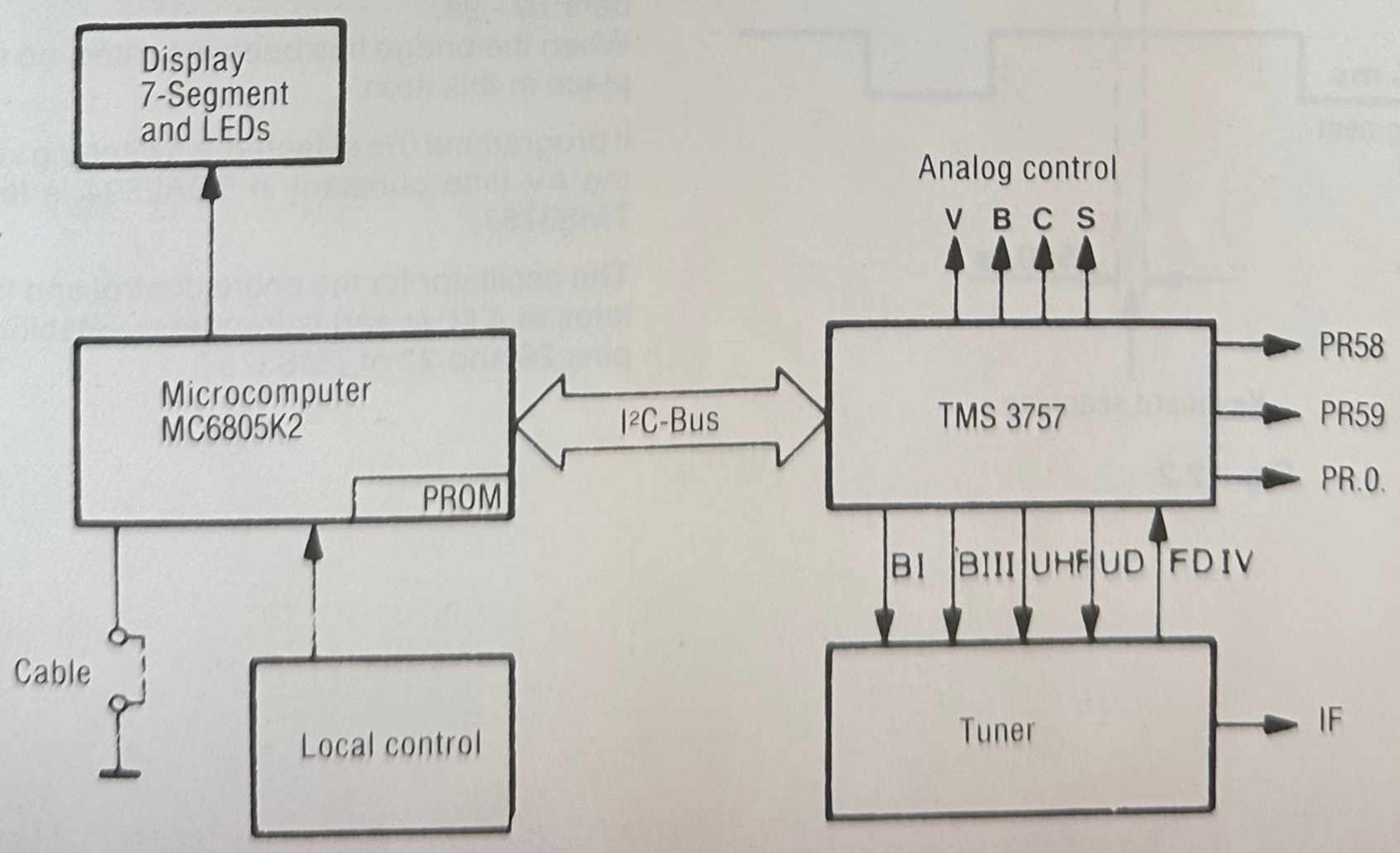


Fig. 12.1

After this, the tuning can be changed, via the fine tuning keys (fine +, fine —), by —4 MHz to +3,875 MHz relative to the CCIR standard frequency, both in the programme and in the channel mode.
This is done in steps of 125 kHz in the desired direction. If one of both keys remains depressed for more than 2 seconds, the speed of the step will increase (to about 8 steps/-sec.). The steps are once again indicated by the 7-segment programme indication, whereby step 32 corresponds with the CCIR standard frequency.
If both keys are depressed simultaneously, the CCIR standard frequency is restored.

12.4 I^2C bus

The I^2C bus is a dual-line bus system consisting of one Data line and one Clock line. This bus system enables the serial and bidirectional communication between various microprocessors and periphery ICs having a specially developed I^2C bus interface. In this way the number of connections is reduced, which leads to a simplified construction of the circuit and to an increased reliability (fewer soldered joints, connections, contacts, etc.).

In the rest position (i.e. no data transmission), both lines lie at high levels via pull-up resistances.
Data transmission is started when the Clock line is "high" (see Fig. 12.3) and a negative flank (H-L) appears on the Data line (start condition). Data evaluation takes place during the H-level of the clock pulses.

The end of the data transmission (stop-condition) is realized by signalling a positive flank (L-H) on the Data line and a simultaneous H-level on the Clock line.

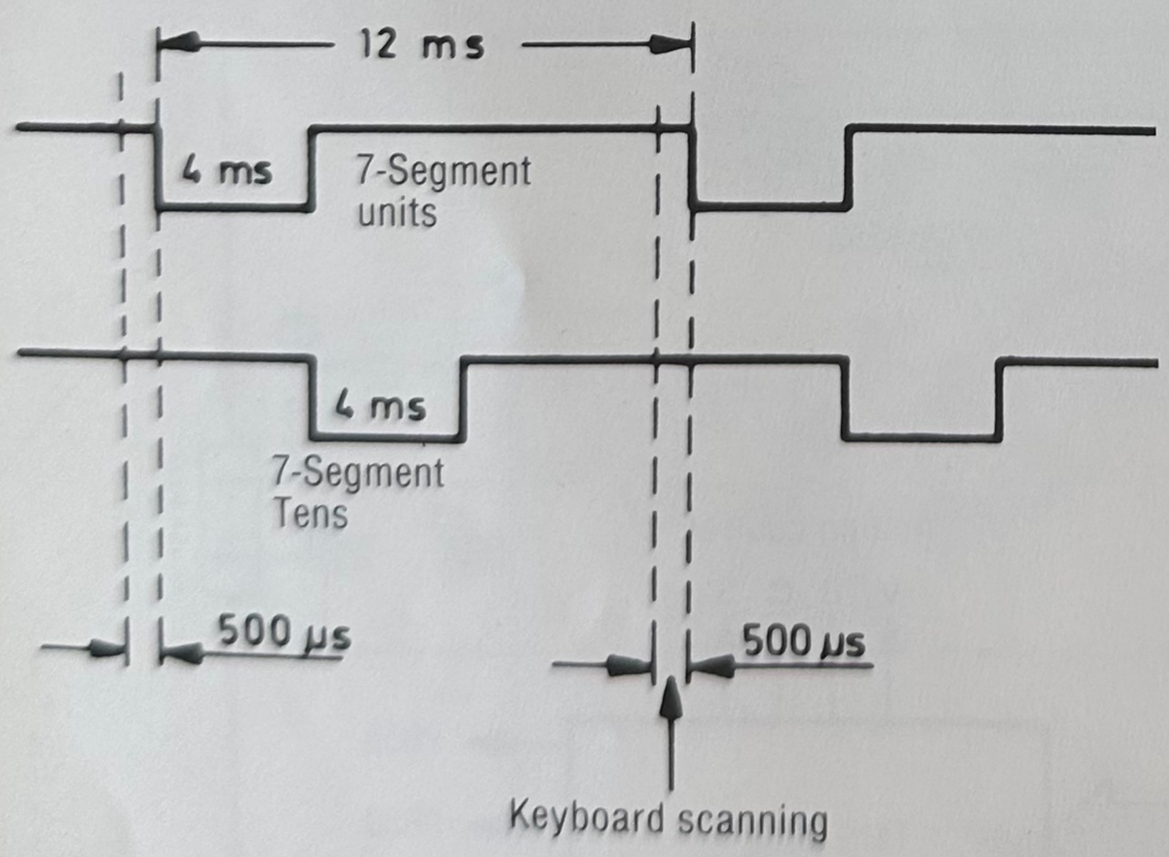


Fig. 12.2

12.5 The acknowledge bit

On the basis of the I^2C bus specification, each address or data byte received is followed by an acknowledgement signal.
To this end, the transmitter, after having transmitted a byte, generates an extra synchronizing pulse. During this period of time, the receiver brings the Data line, which was brought to H-level by the transmitter IC, to L-level. Dependent upon the structure of the data input in "Wired-and-Technik", the transmitter IC soon receives notice as to whether the data have been stored. An exeption is the answer bit after the start byte. In this case the Data line is not put to L-level by the receiver, for no receiver address has been supplied yet ("Dummy" acknowledge). If reception of the information is not ackowledged, the transmitter IC repeats the information.

12.6 Search tuning

Search tuning starts from the channel number adjusted.
The microcomputer adjusts the analogue outputs of sound intensity and brightness for minimum values and feeds out the CCIR standard frequency of the next channel.
If at this frequency no transmitter is identified that can be received well, step-wise scanning of the channel pattern takes place. When the channel pattern has been passed through and no transmitter has been found, the search tuning is followed from the next higher channel.
If a television transmitter is received, however, the HCOIN line (MC input PC4) is put to L-level and search tuning is interrupted. After a delay time of 400 ms the microcomputer switches the sound intensity and the brightness back to the original values.

12.7 Storage

After depressing the storage key, the channel number tuned to, fine tuning and all analogue values are stored into the PROM in binary form.
60 programmes and a maximum of 8 analogue values can be stored, but at the moment only brightness, saturation, contrast and sound intensity are stored. Contrast cannot be remote controlled, but only at the set itself.
The analogue values are always fixed for all programme locations at the same time by the last operation of the storage key.
By depressing a programme number, the transmitters stored in the memory can be called and, by entering the channel mode, transmitters can be selected direct via their channel numbers.
S-channels can only be received when input PC 3 lies at H-level and the service bridge to ground has not been mounted. The S-channels are numbered with the channel numbers 70 - 99.
When the bridge has been mounted, no search tuning takes place in this area.

If programme 0 is selected, a switching voltage for switching the AV time constant in TDA2594 is fed out on pin 18 of TMS3757.

The oscillator for the entire control and tuning system oscillates at 4 MHz and is frequency-stabilized via a crystal on pins 26 and 27 of TMS3757.

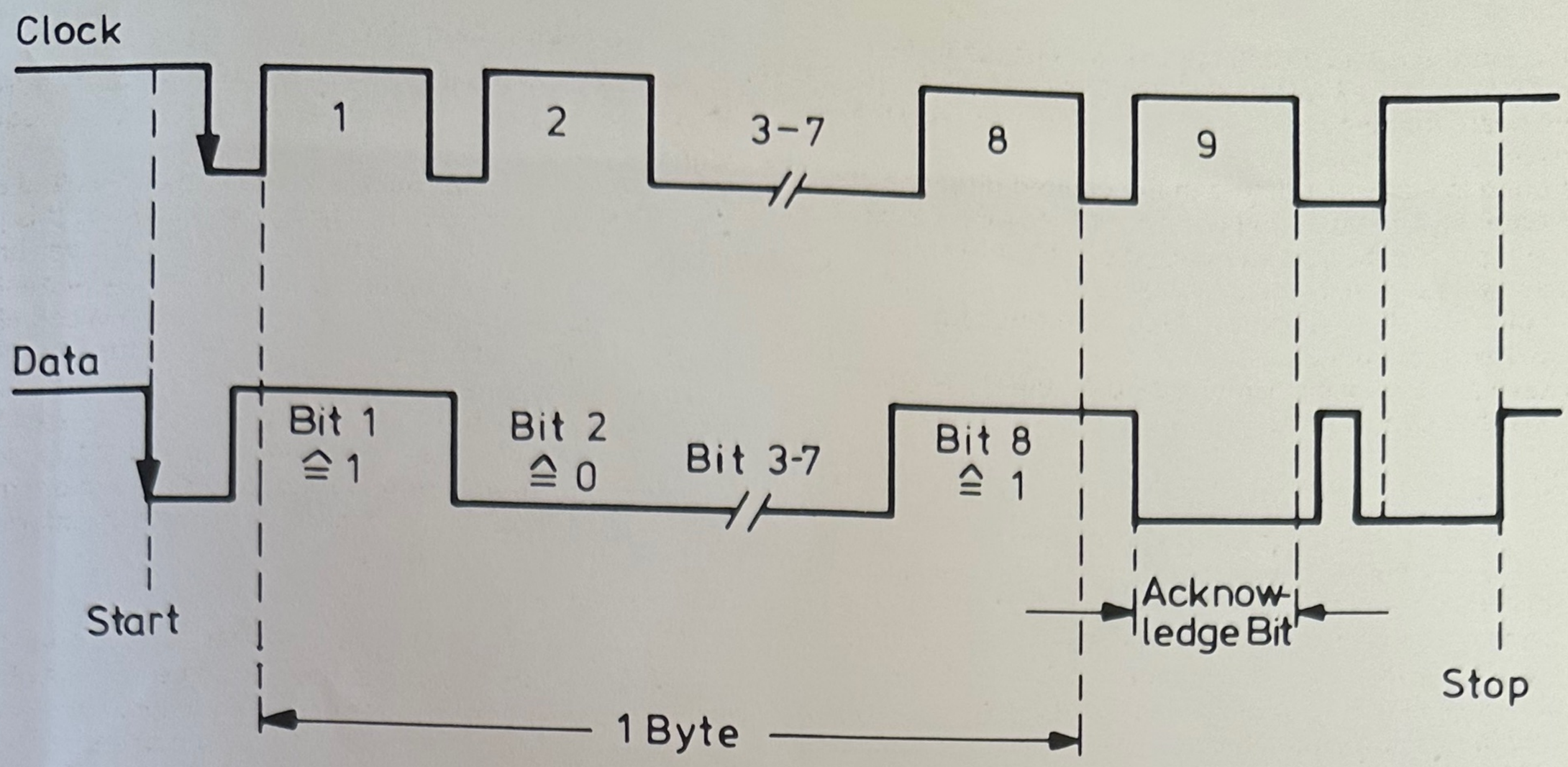

Clock
1
2
3–7
8
9
Data
Bit 1
≙ 1
Bit 2
≙ 0
Bit 3-7
Bit 8
≙ 1
Start
Acknow-
ledge Bit
Stop
1 Byte

Fig. 12.3